Amendments to the Claims:

This Listing of Claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (Currently Amended) A system for synchronizing the clock frequencies of power processing devices and digital signal processing devices in an electronic system comprising :

[a clock;]

a pulse width modulated power processing device; and

a digital signal processor having a clock for use in said digital signal processor operational clock frequency;

wherein said pulse width modulated power processing device is communicatively coupled to said clock within said digital signal processor;

[wherein said digital signal processor is communicatively coupled to said clock;]

wherein said pulse width modulated power processing device [and said digital signal processor use] uses said clock within said digital signal processor for [their] its operational clock [frequencies] frequency..

2. (Original) A system according to claim 1, wherein the power processing device is a pulse width modulated power amplifier.

3. (Original) A system according to claim 1, wherein the power processing device includes a pulse width modulated power supply.

4. (Original) A system according to claim 3, wherein the power processing device provides power to the digital signal processor.

5. (Original) A system according to claim 3 wherein the power processing device further includes a pulse width modulated power amplifier.

6. (Original) A system according to claim 5 wherein the pulse width modulated power supply provides power to the pulse width modulated power amplifier and the digital signal processor.

7. (Original) A system according to claim 1 wherein the clock operates at 96kHz.

8. (Original) A system according to claim 5, wherein the pulse width modulated power amplifier drives a loudspeaker.

9. (Original) A system according to claim 1, wherein the clock has a clock frequency that is used by the digital signal processor.

10. (Original) A system according to claim 9, wherein the digital signal processor uses a multiple of the clock frequency for its operation.

11. (Original) A system according to claim 9, wherein the digital signal processor uses an integer fraction of the clock frequency for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

12. (Original) A system according to claim 9, wherein the digital signal processor uses integer related derivatives of the clock frequency for its operation.

13. (Original) A system according to claim 1, wherein the clock has a clock frequency that is used by the pulse width modulated power processing device.

14. (Original) A system according to claim 13, wherein the pulse width modulated power processing device uses a multiple of the clock frequency for its operation.

15. (Original) A system according to claim 13, wherein the pulse width modulated power processing device uses an integer fraction of the clock frequency for its operation.

16. (Original) A system according to claim 13, wherein the pulse width modulated power processing device uses integer related derivatives of the clock frequency for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

17. (Original) A system for synchronizing the clock frequencies of power processing devices and digital signal processing devices in an electronic system comprising :

a pulse width modulated power supply;

a pulse width modulated power amplifier; and

a digital signal processor, including:

a clock;

wherein said pulse width modulated power supply is communicatively coupled to said clock in said digital signal processor;

wherein said pulse width modulated power amplifier is communicatively coupled to said clock in said digital signal processor;

wherein said digital signal processor and said pulse width modulated power supply and said pulse width modulated power amplifier use said clock in said digital signal processor for its operational clock frequency.

18. (Original) A system according to claim 17, wherein the pulse width modulated power supply provides power to the pulse width modulated power amplifier and the digital signal processor.

19. (Original) A system according to claim 17, wherein the clock in said digital signal processor operates at 96 kHz.

20. (Original) A system according to claim 17, wherein the pulse width modulated power amplifier drives a loudspeaker.

21. (Currently Amended) A method for synchronizing the clock frequencies of power processing devices and digital signal processing devices comprising the steps of:

using a clock within a digital signal processor (DSP) to operate [a digital signal processor (DSP)] the DSP; and

using the clock within the DSP to operate a pulse width modulated (PWM) power processing device.

22. (Cancelled).

23. (Original) A method according to claim 21, wherein the PWM power processing device is a PWM power amplifier.

24. (Original) A method according to claim 21, wherein the PWM power processing device is a PWM power supply.

25. (Original) A method according to claim 24, wherein the PWM power supply provides power to the DSP and to a PWM power amplifier.

26. (Original) A method according to claim 21, wherein:

the DSP has an input and an output; and

the PWM power supply processing device has an input and an output.

27. (Original) A method according to claim 26, wherein the output of the DSP feeds the input of the PWM power supply.

28. (Original) A method according to claim 26, wherein the output of the PWM power supply feeds the power input of the DSP.

29. (Original) A method according to claim 23, wherein the PWM power amplifier drives a loudspeaker.

30. (Original) A method according to claim 23, wherein the PWM power amplifier drives a computer.

31. (Original) A method according to claim 21, wherein the clock has a clock frequency that is used by the DSP.

32. (Original) A method according to claim 21, wherein the clock has clock frequency that is used by the PWM power processing device.

33. (Original) A method according to claim 32, wherein the PWM power processing uses a multiple of the clock frequency for its operation.

34. (Original) A method according to claim 31, wherein the DSP uses a multiple of the clock frequency for its operation.

35. (Original) A method according to claim 21, wherein the clock operates at 96 kHz.

36. (New) A system for synchronizing the clock frequencies for an audio electronic device, the system comprising:

a digital signal processor (DSP) having a clock adapted to provide clock frequency for the operation of the DSP;

a pulse width modulated power supply communicatively coupled to the clock in the DSP;

a pulse width modulated power amplifier communicatively coupled to the clock in the DSP;

wherein the pulse width modulated power supply and the pulse width modulated power amplifier use the clock in the DSP for their respective operational clock frequency.

37. (New) The system according to claim 36, wherein the pulse width modulated power supply uses an integer multiple or integer fraction of the clock frequency of the clock within the DSP for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

38. (New) The system according to claim 36, wherein the pulse width modulated power amplifier uses an integer multiple or integer fraction of the clock frequency of the clock within the DSP for its operation so that the sum and difference frequencies fall outside of the audible frequency range.